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A MICROPROCESSOR-BASED BI'' ERROR PERFORMANCE MONITOR.(U)
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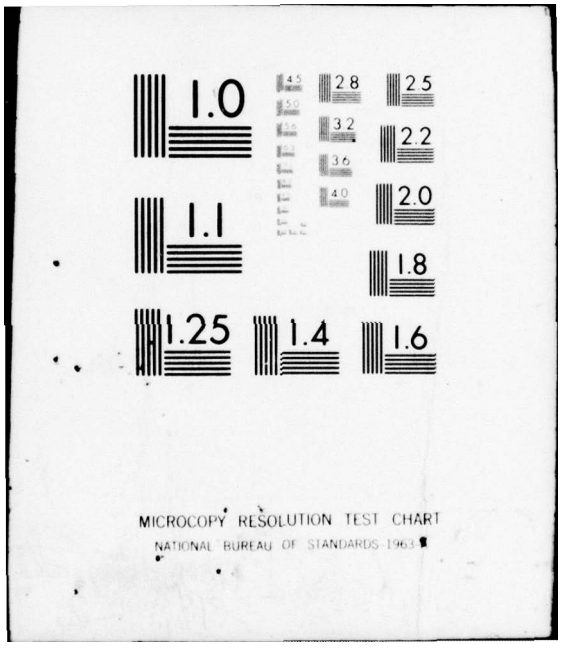
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1.1
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1.4
1.6
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2.0
2.2
2.5
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MICROCOPY RESOLUTION TEST CHART
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Microprocessor
Digital Communication
General Purpose Interface Bus
Digital Error Parameters
Percent Error Free Seconds
Bit Error Rate

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes one approach in realizing a digital communication system performance monitor which utilizes microprocessor technology and selected algorithms to process and display bit error parameters based on detected errors in a digital communication system.

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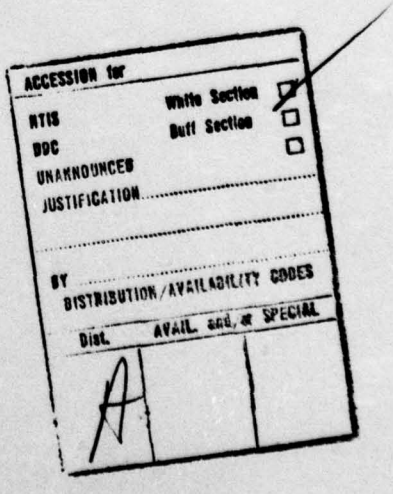
TABLE OF CONTENTS



LIST OF ILLUSTRATIONS

1.0 INTRODUCTION.

The problem of defining meaningful error parameters as well as associated digital performance assessment equipment is a growing concern in the world of digital communications. Error parameters are generally calculated on the basis of the number of errors counted over a defined time interval. From this information, parameters such as Bit Error Rate (BER), Percent Error Free Seconds (%EFS), Percent Availability, and others can be calculated. The time interval over which errors are observed also determines the statistical confidence in the various parameters calculated. Performance monitoring equipment should provide the ease and flexibility needed to determine several different parameters since each error characteristic has a different impact on the service to the user.

With the advent of the microprocessor (μp), a viable, low-cost capability for implementation of effective error-computation algorithms is now realizable. Also, by utilizing a microprocessor-based monitor, different performance parameters can be processed simply by changing software subroutines within the monitor.

This report describes the methodology used to implement a prototype monitor which utilizes microprocessor technology to derive several error parameters and provide a digital communication system performance assessment capability.

2.0 MONITOR REQUIREMENTS AND DESIGN PHILOSOPHY.

Voice channel noise characteristics in a digital system differ from those of an analog system with regard to system degradation. While graceful degradation occurs in analog systems, user quality remains relatively constant in digital systems until a noise threshold is reached whereby the multiplexer is no longer able to decode the digital information (Figure 2). At this point, several magnitudes of error performance are realized within just a few decibels of receive signal level (Figure 3). Thus, the requirement for a monitor with sensitive error parameters to assess system degradation is readily apparent.

The prototype monitor (Figure 1) uses microprocessor technology to process several selectable error parameters on the basis of clock and error inputs. These inputs are obtained from a station clock and time division multiplexer (TDM) error output, respectively. Each error parameter is selectable by means of a front panel "mode" switch and is displayed on an analog meter with a scale indicating decades of error performance. Front panel alarm indicators inform the user of error performance. Each threshold or zone is preset or varied at any time by a front panel control. The monitor continually processes all parameters but displays only the parameter selected from the front panel. By utilizing a front panel analog meter, the user can determine the relative system integrity at a glance.

FIGURE 1
PROTOTYPE MONITOR

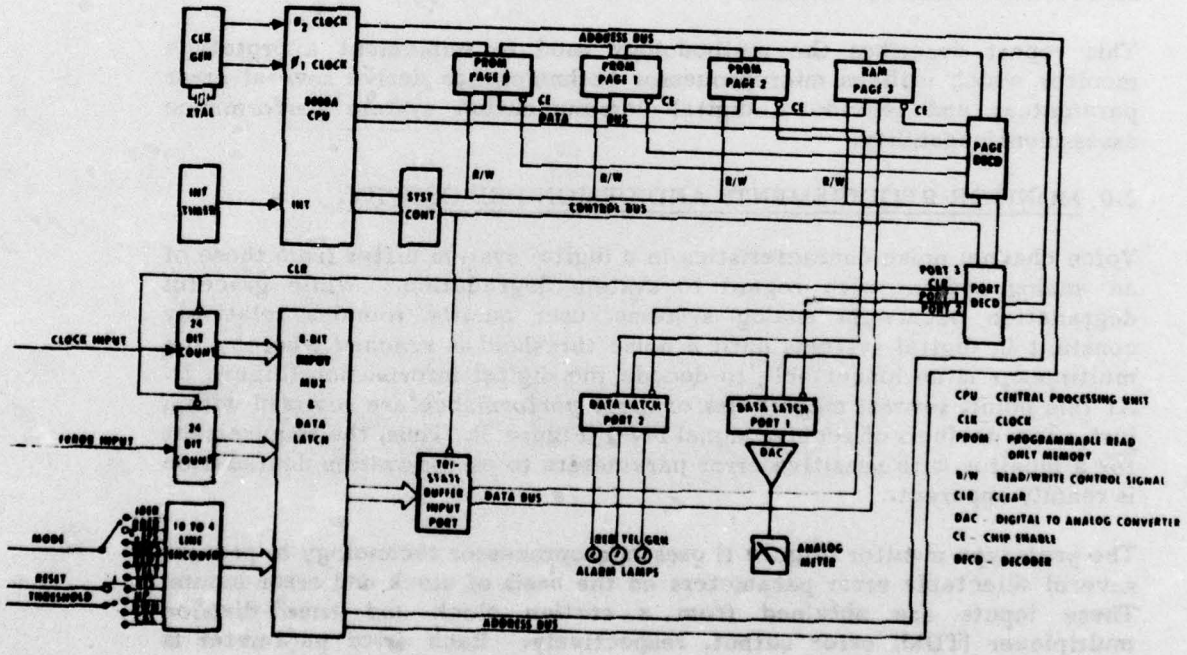


FIGURE 4
MONITOR BLOCK DIAGRAM

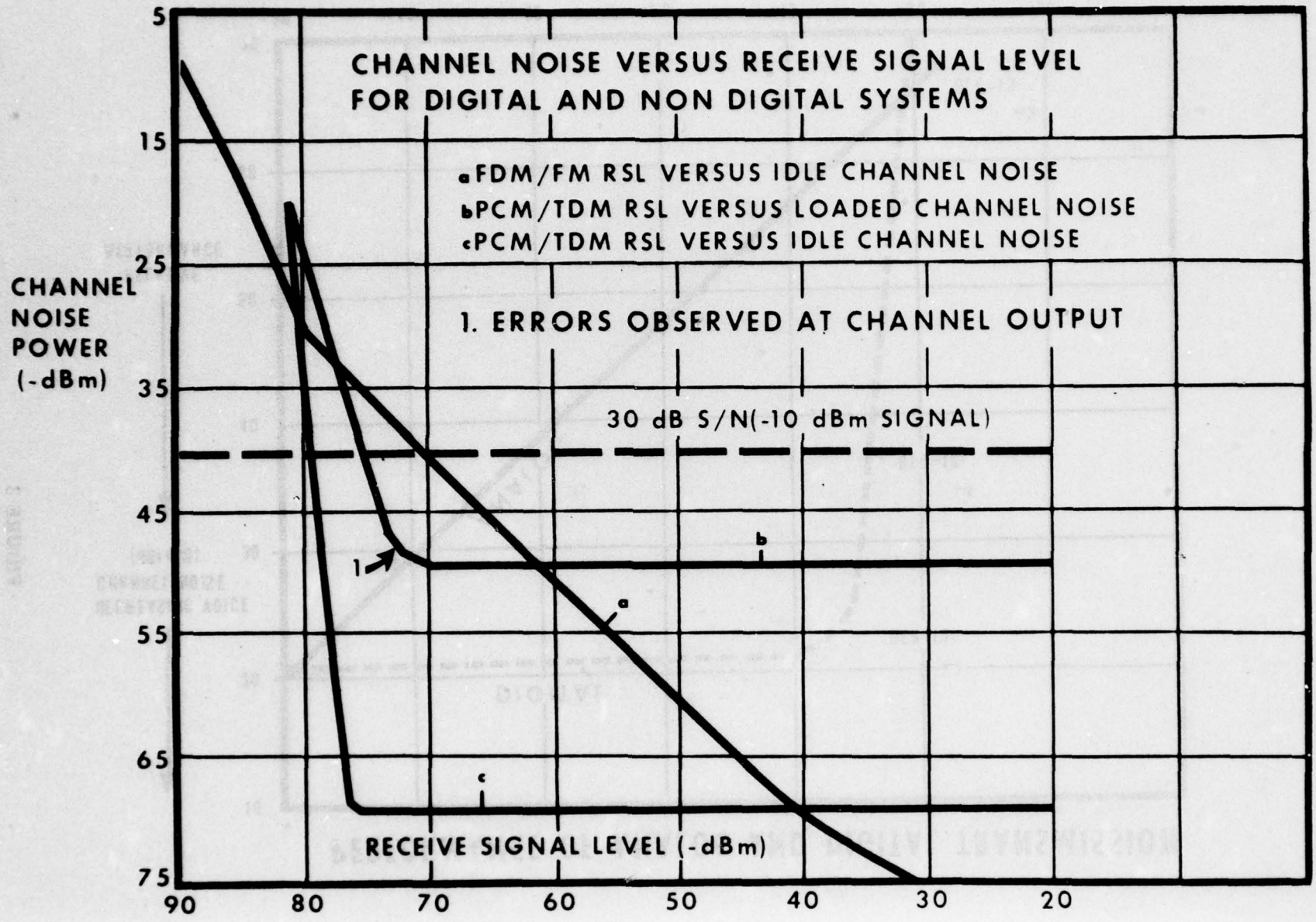

CHANNEL NOISE VERSUS RECEIVE SIGNAL LEVEL
FOR DIGITAL AND NON DIGITAL SYSTEMS
aFDM/FM RSL VERSUS IDLE CHANNEL NOISE
bPCM/TDM RSL VERSUS LOADED CHANNEL NOISE
cPCM/TDM RSL VERSUS IDLE CHANNEL NOISE
1. ERRORS OBSERVED AT CHANNEL OUTPUT
30 dB S/N(-10 dBm SIGNAL)
CHANNEL NOISE POWER (-dBm)
RECEIVE SIGNAL LEVEL (-dBm)
5
15
25
35
45
55
65
75
90
80
70
60
50
40
30
20
a
b
c
1

FIGURE 2

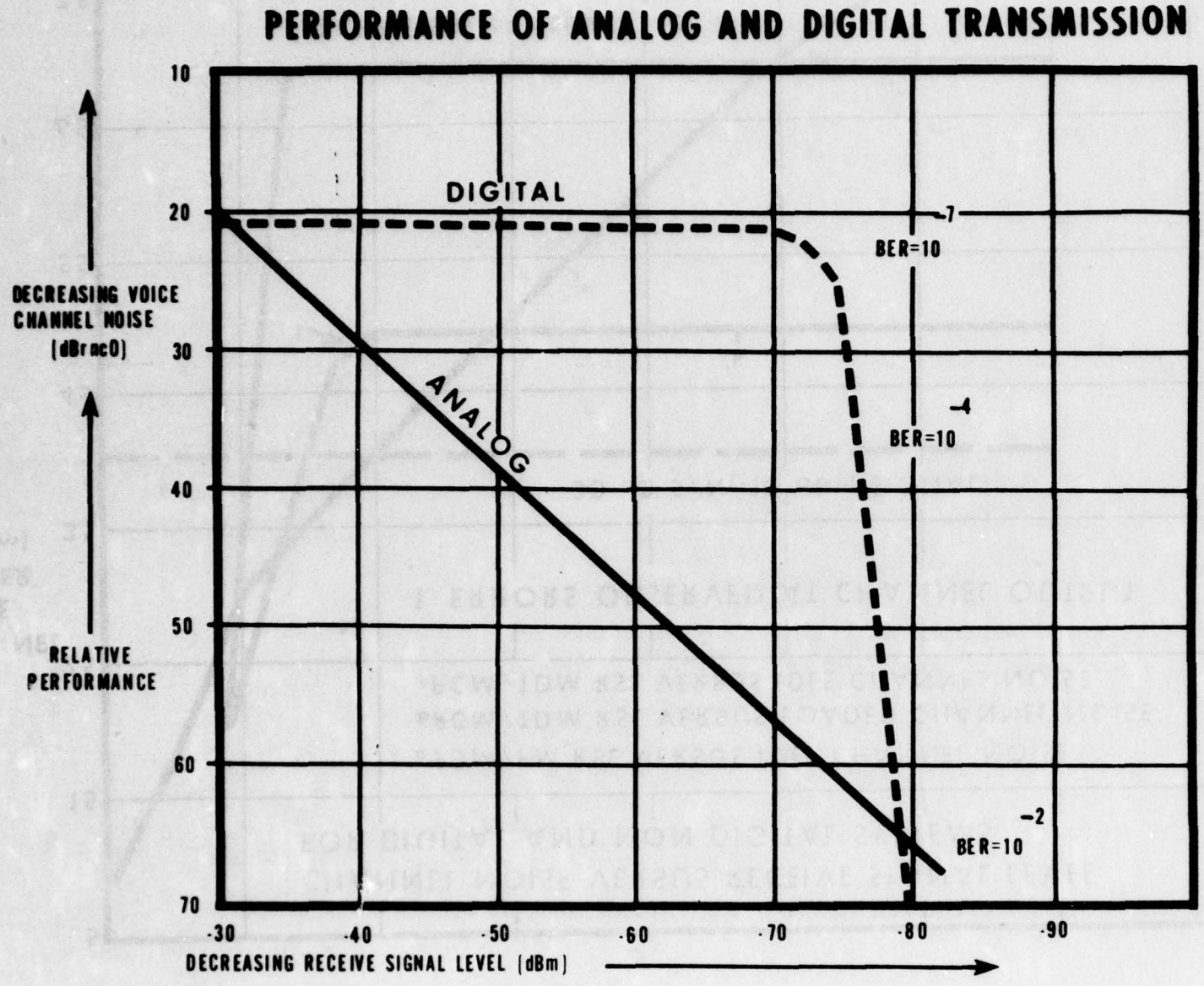

PERFORMANCE OF ANALOG AND DIGITAL TRANSMISSION
DIGITAL
ANALOG
BER=10^-7
BER=10^-4
BER=10^-2
DECREASING VOICE CHANNEL NOISE (dBrnc0)
RELATIVE PERFORMANCE
10
20
30
40
50
60
70
-30
-40
-50
-60
-70
-80
-90
DECREASING RECEIVE SIGNAL LEVEL (dBm)

FIGURE 3

This is done by comparing the pointer position with the meter scale endpoints, thus obtaining a relative indication without even looking at the scale markings. For a more accurate indication, the meter value can be taken from a digital storage register for use by a monitoring computer or for use in a digital display. An interface is presently under development to make the monitor controllable by the General Purpose Interface Bus (GPIB) (GPIB - IEEE STD 488-1975)(See Appendix). This will provide monitor functions and data transfer from a remote location making the monitor suitable for use in remote communication sites.

3.0 DIGITAL ERROR ALGORITHMS AND SOFTWARE DESCRIPTION.

There are many error parameters being considered for use in digital communications systems. A few of these are: (1) Percent Error Free Seconds (%EFS); (2) Percent Availability; (3) Bit Error Rate (BER), etc. The bit error monitor allows the user to simultaneously evaluate several of these parameters and to change parameters, if needed. Error algorithms are implemented in programmable read only memory (PROM). These algorithms cause input ports to be sampled periodically in order to obtain clock and error pulse information. The inputs serve as arguments for error parameter subroutines (see arithmetic subroutines) which return the calculated parameter values to the appropriate registers. The value in the respective register is then converted to a proportional analog voltage by the digital-to-analog converter (DAC) and is displayed by the front panel meter.

Three parameters were selected for evaluation in the prototype monitor. These are: (1) Instantaneous Bit Error Rate (IBER); (2) Recursive Bit Error Rate (RBER); (3) Percent Error Free Seconds (%EFS)(see monitor functions) and are explained in more detail in Section 6.0.

The Central Processing Unit (CPU) has a two microsecond instruction cycle time, eight programmable registers, push-down stack, and 160 operation codes or instructions. The program is driven by the interrupt timer. Each quarter second, an interrupt signal from the interrupt timer causes an interrupt routine to be called. On three of every four calls, only the UP/DOWN threshold switch is checked for change in status. Once every second, the entire program is executed - i.e., input (μp samples counter values), computation of the recursive BER, computation of %EFS, selection of the proper mode, and output of the corresponding values. The push-down stack is utilized extensively to allow the subroutines to use the internal μp registers and then return to the main program with the original register values intact. All arithmetic subroutines are stored on memory page two Programmable Read Only Memory (PROM) and they manipulate data stored on page three Random Access Memory (RAM). The subroutine arguments are data buffer locations and both the addresses and the counter values are passed into the subroutines via the input multiplexer.

In the following text, two arithmetic subroutines are discussed to show how error algorithms are realized in the monitor. The recursive algorithm for computation of the mean is used to calculate the RBER parameter while the binary logarithm algorithm is used in the output cycle to display decades of error performance on a linear analog meter.

4.0 SYSTEM DESCRIPTION.

In the simplified block diagram shown in Figure 4, two 24 bit counters accumulate clock and error pulses over a specified time interval determined by the interrupt timer. The positions of ten possible front panel switch settings are encoded through a ten-to-four line encoder providing a binary coded decimal (BCD) representation of the desired mode of operation and threshold values. The data output of the counters and the ten-to-four line encoder are then multiplexed into eight bit bytes and are gated onto the data bus upon command from the microprocessor. The eight bit byte selected is determined by the address sent to the multiplexer from the μp via the address bus. Program storage is done on three pages (256 bytes per page) of PROM with one page of RAM being used for data storage. On every interrupt command (once per second), each byte sampled from the counters and encoder is stored in designated RAM locations. The system software then operates on the data stored in RAM and utilizes multiple byte processing on a single byte processor to calculate each error parameter and return the value to memory (RAM). The parameter value is then sent to the digital-to-analog converter (DAC) through a data latch (Port 1) and the parameter value is displayed on an analog meter. In a like manner, the parameter value is compared with error threshold value located in RAM. If the parameter value exceeds an error threshold value, an alarm byte is sent to a data latch (Port 2) and the appropriate alarm lamp is activated. Any reference made to a third port, by the μp, generates an asynchronous clear pulse to the two counters. Error threshold values are set by the threshold switch on the front panel. Holding the switch in the "UP" position slowly increments the threshold value and displays that value on the meter. Similarly, depressing the switch into the "DOWN" position decrements the threshold until the switch is released. The front panel reset button clears all counters and starts the main program.

5.0 MONITOR FUNCTIONS.

The following functions and error parameters can be initiated by the front panel "MODE" switch or "THRESHOLD" switch:

IBER - (Instantaneous Bit Error Rate Mode). The value of the error counter is divided by the value of the clock counter once each second. The quotient is stored in RAM and displayed on the meter as a BER value, e.g., 1×10^{-7}.

RBER - (Recursive Bit Error Rate Mode). RBER is calculated by recursively combining the current sample of IBER with all previous samples to obtain a long-term mean BER (See Arithmetic Subroutine - recursive algorithm for computation of the mean). The effective sample duration in this mode is the elapsed time from the time the front panel reset was last depressed to the present time. This interval may be from one second to six months. The meter reading is continuously updated to reflect the mean BER.

%EFS - (Percent Error Free Second Mode). The time duration of the previous error free transmission block divided by the total time of observation from front panel reset to present is displayed on the meter as a percentage, e.g., 99.9. The number of seconds since the previous error and the error before that one is displayed rather than the time since the previous error (Figure 5).

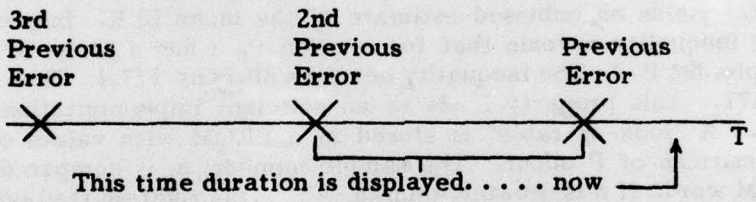


FIGURE 5

NBPS - (Number of Bits Per Second Mode). The value of the clock counter used to evaluate error parameters is displayed on the meter and provides a convenient indication of sample size. This value is based on the number of clock bits accumulated over a one second interval.

CAL - This mode provides a lamp test (activates all lamps) and a full scale meter deflection for calibration purposes.

REDT - (Red Threshold Mode). In this mode, the current value of the "Red" error threshold is displayed on the meter. The UP/DOWN switch is activated to allow the operator to change the threshold if desired.

YELT - (Yellow Threshold Mode). The current value of the "Yellow" error threshold is displayed on the meter. The UP/DOWN switch is activated to allow the operator to change the threshold, if desired.

6.0 ARITHMETIC SUBROUTINES.

The following algorithms are implemented as software subroutines:

Recursive Algorithm for Computation of the Mean[1]

If the number of bits in error in the i-th count interval is a random variable, e_i, then the mean BER, μ_n, over a count interval is:

$$\mu_n = \frac{1}{n} \sum_{i=1}^{b} e_i \qquad (1)$$

Recursive computation of the mean can be obtained from:

$$\mu_n = \mu_{n-1} + \frac{1}{n} (e_n - \mu_{n-1}) \qquad (2)$$

Implementation of division by n is difficult and slow, hence, the algorithm proposed by Aninoff, et al[1], is employed in equation (2). Division by n is replaced by division by 2P. This is implemented by right shifting P times the quantity $(e_n - \mu_{n-1})$. The optimal algorithm ($2<n<10^6$) selects P such that the inequality

$$1.3863(2^{P-1})<n<1.3863(2^P). \qquad (3)$$

is satisfied. The substitution of the algorithm proposed by Aninoff, et al, in equation (2) yields an unbiased estimate of the mean BER. Inspection of the above inequality reveals that for a given P, n has a range of values. For example, let P=7. The inequality becomes $88.7<n< 177.4$. Then for P=7, n=89 to 177. This property leads to an efficient implementation of the algorithm. A "look-up table" is stored in a PROM with values of n for which transitions of P occur. The sample number, n, is compared to the first PROM word. If n is greater, then $(e_n - \mu_{n-1})$ is right-shifted again. The process is repeated until n is not greater than the next PROM word. Shifting is then terminated and $(e_n - \mu_{n-1})$, which has been right-shifted P times, is added to μ_{n-1} to obtain an estimate of the mean BER, μ_n.

Algorithm for Computation of Binary Logarithm[2]

Hall, et al[2], have represented $\log_{10}N$, where N is a binary number, defined as:

$$N = 2^k(1+x) \qquad (4)$$

and k is an integer with $0<x<1$. The $\log_2 10$ is a conversion constant, hence, the $\log_2 N$ algorithm is the unknown. Since $N = 2^k(1+x)$, then:

$$\log_2 N = k + \log_2(1 + x) \qquad (5)$$

where the first term is the characteristic and the second term is the mantissa. The characteristic, k, can be determined exactly by setting the length of N (power of 2 for the most significant bit (MSB)) into a count register. This is implemented by decrementing the count register while left shifting N (in the mantissa register) until a one is encountered in the MSB of the mantissa register.

For example:

	2^{11}	.	.	.	.	.	2^{5}	.	.	.	2^{1}	2^{0}
N =	0	0	0	0	0	0	1	0	1	1	0	0
count =	11	10	9	8	7	6	5	4	3	2	1	0

Starting from eleven, the count would be decremented to five, where the first one (1) in N is encountered and the shifting stops.

7.0 TERMINAL EQUIPMENT CONFIGURATION AND SYSTEM MONITORING POINTS.

Both clock and error inputs require a standard TTL format. In the terminal equipment configuration (Figure 6), two methods can be utilized to supply the necessary inputs and signal format. The first method is an out-of-service technique which involves the use of one T1 port of the second level multiplexer. A pseudo-random bit stream in T-1 format is generated and inserted into the mission traffic via the selected multiplexer port. The pseudo-random pattern is then demultiplexed at the receive end of the link in test. The pattern is then checked for errors against the same pseudo-random pattern which was generated. These errors and the station clock provide the necessary inputs to the monitor. A second method (Figure 7), involves the use of pseudo errors detected at the multiplexer slicers as an input to the monitor. Since the pseudo error rate runs roughly parallel to the actual mean BER and provides a quicker indication of system degradation, this method is preferred. Additionally, this is an in-service technique and is easily implemented in the second level multiplexer.

8.0 MONITOR APPLICATIONS.

A General Purpose Interface Bus (GPIB), IEEE STD 488-1975 (Appendix) adapter is presently under development at the USAF Academy. With the addition of the adapter, the monitor will be remotely programmable and controllable for use at remote unmanned communication sites or with any site controller which is GPIB compatible. For example, monitor functions such as IBER, RBER, %EFS, etc can be selected and sampled by a calculator or computer-based test system. The monitor also has the advantage of on-site data preprocessing which can eliminate needless processing by the master data acquisition device at a distant terminal station.

9.0 CONCLUSION.

At the present time, the search continues for statistically meaningful error parameters in the digital world. The microprocessor-based bit error monitor described in this report provides the ease and flexibility needed to implement new error parameters as they are developed. Additionally, the

monitor has the capability to calculate several parameters simultaneously which provides the user with both long and short term error performance parameters. The use of microprocessor technology in the monitor also provides an extremely cost effective approach in implementing the computational capability required to process error parameters. The monitor provides a viable solution to some of the problems encountered in digital communication system performance monitoring and has great promise for future performance monitor requirements.

Terminal Equipment Configuration

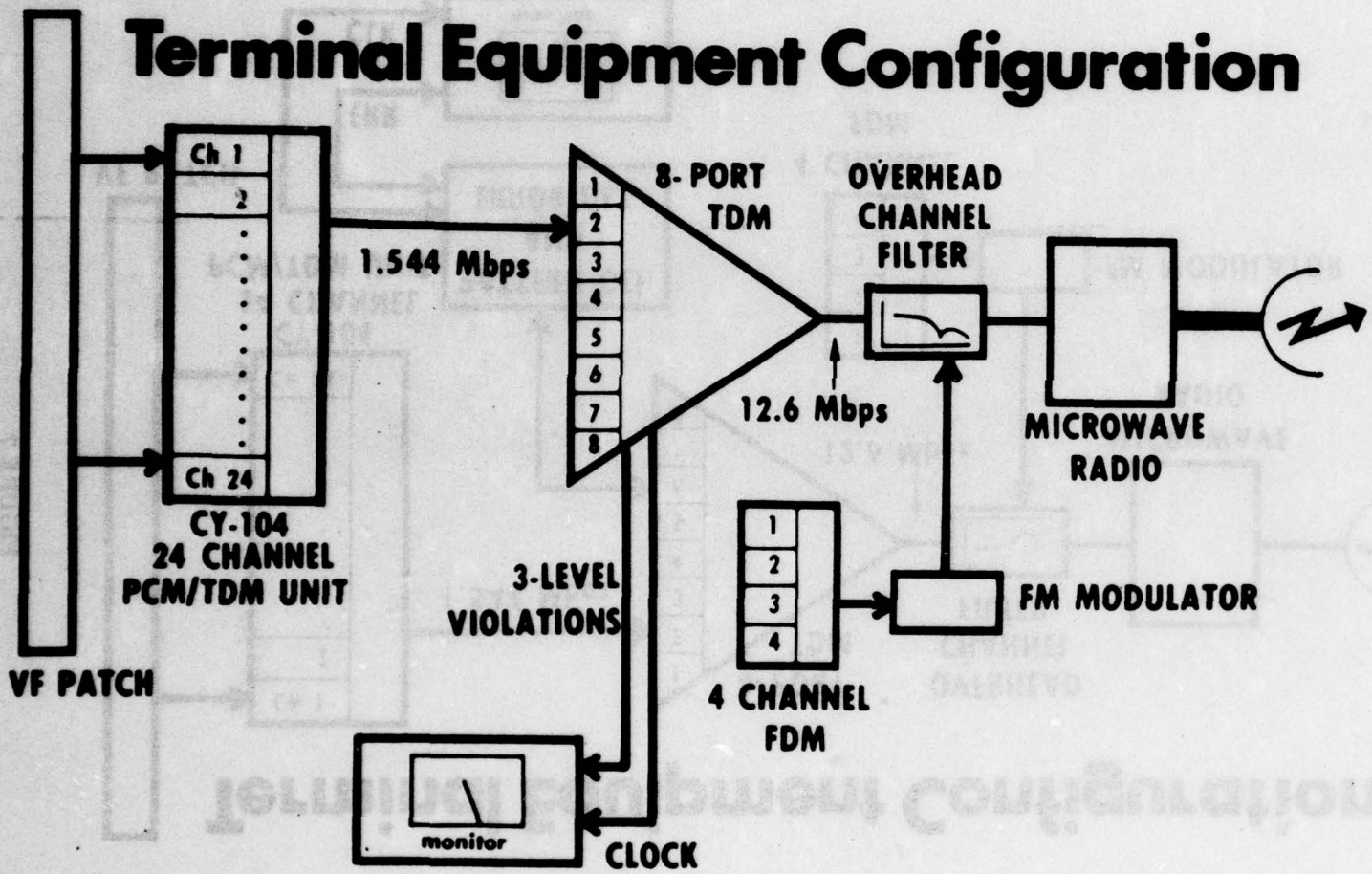


FIGURE 6

Terminal Equipment Configuration

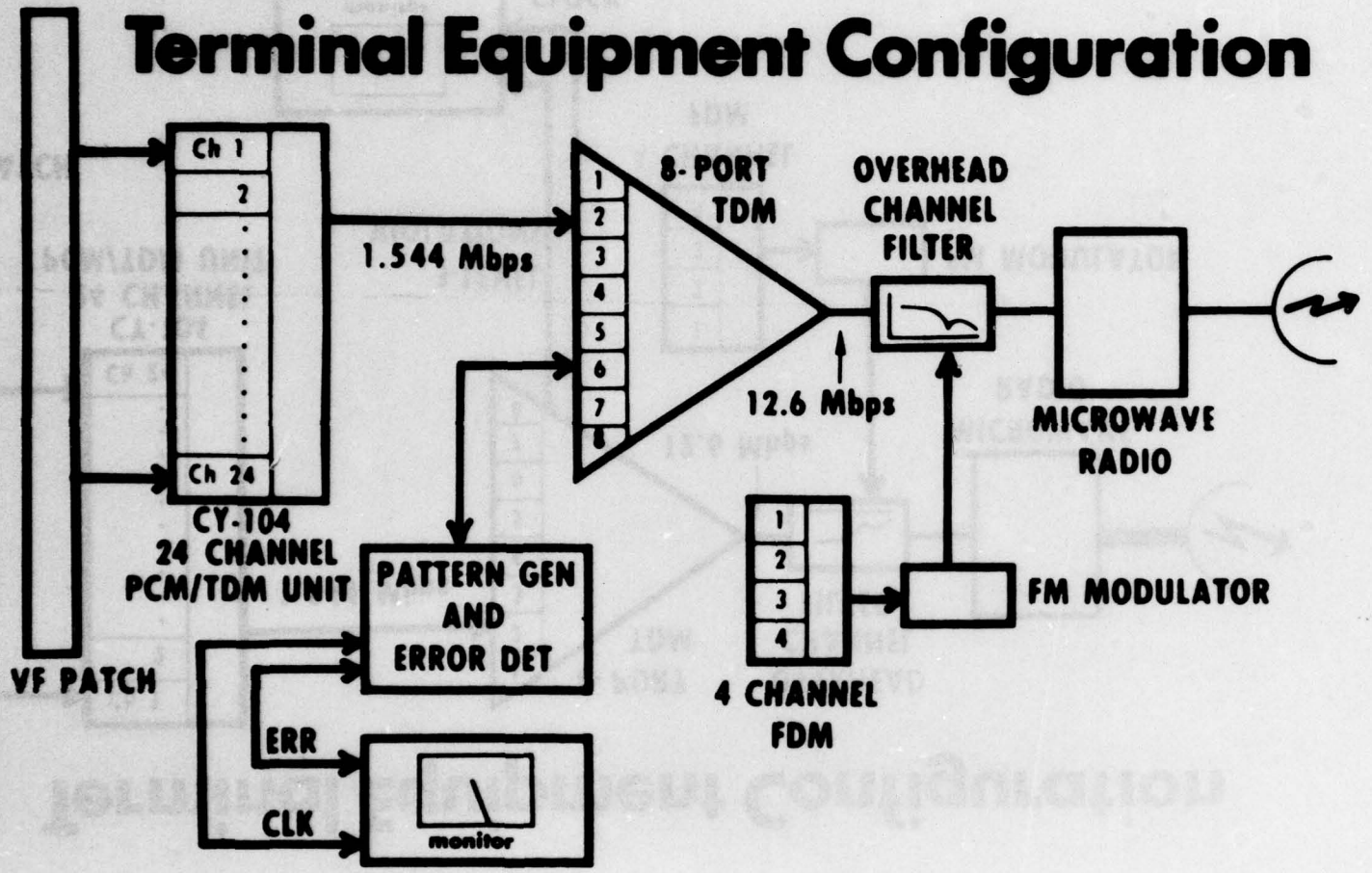


FIGURE 7

APPENDIX
GENERAL PURPOSE INTERFACE BUS DESCRIPTION

The overall purpose of an interface system is to provide an effective communication media so that two or more devices or systems can transmit meaningful messages between each other. The IEEE STD 488-1975 Standard Digital Interface for Programmable Instrumentation is such an interface. This interface will be referred to as a General Purpose Interface Bus (GPIB) throughout the rest of this paper.

The bus is made up of 16 lines to carry information between instruments connected to the GPIB. Figure 8 gives a pictorial representation of the GPIB. The 16 lines can be divided into three functional groups.

Eight lines are used to transfer data between devices in ASCII coded bit parallel, byte serial format. Other information codes could be used for device dependent messages, however, and the ASCII code is not required by the IEEE standard.

Three lines are dedicated to the control of data byte transfers between devices and are commonly called handshake lines, thus allowing the data to be transferred asynchronously over the GIPB. See Figure 10.

Five additional lines are used for general interface management. One line is used to determine the data mode or the command (addressing) mode for the eight data lines. See Figure 8 for the purpose of each.

Since it takes more than just the physical interconnection of black boxes to have an effective communication media, specific interface functions must be defined. Ten different possible functions are shown in Figure 9 as defined by the standard. The list gives a general idea of the purpose of each function. A description of each function as it relates to hardware can be found in more detail in the IEEE Standard 488-1975. The handshake functions, however, are what make the GPIB a viable interface and are best described by the flow diagram in Figure 10.

For any given device, only those functions required to satisfy the operation of the device need to be included in the design of an instrument.

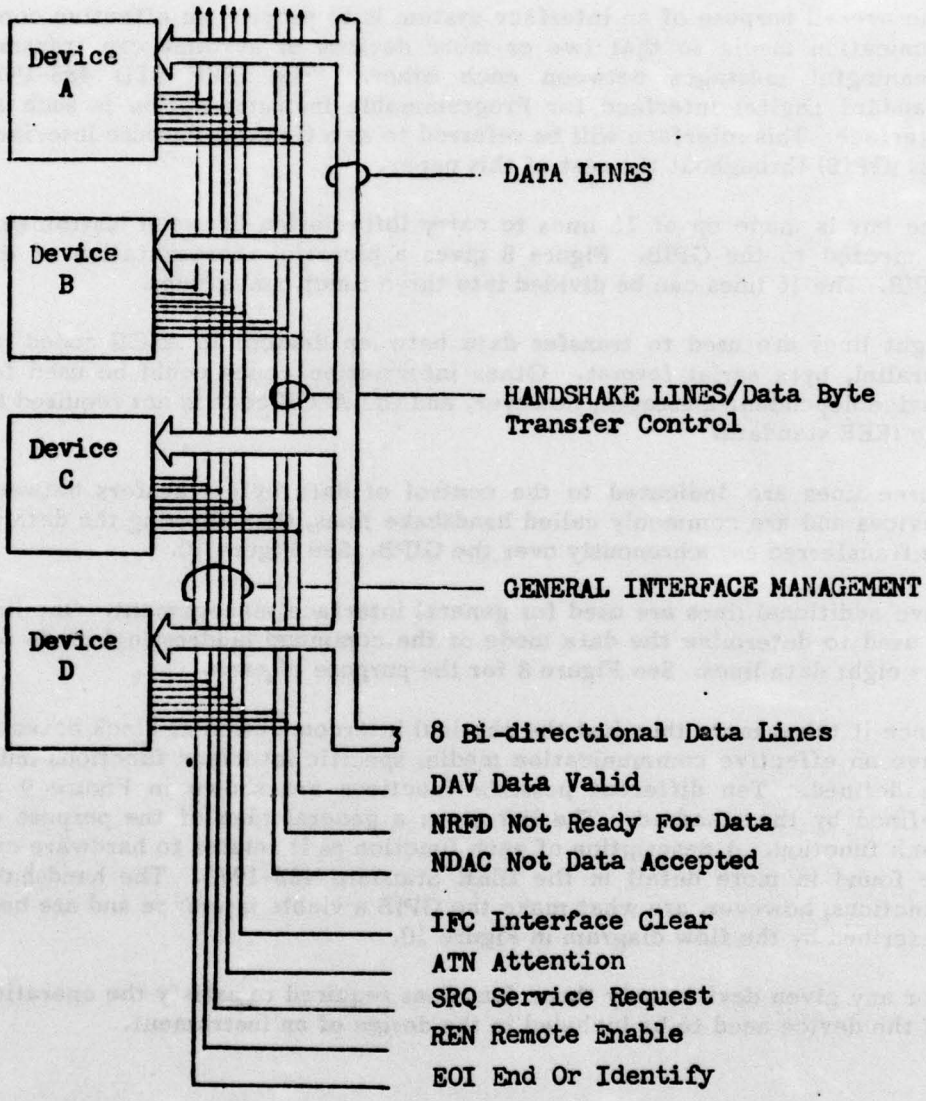
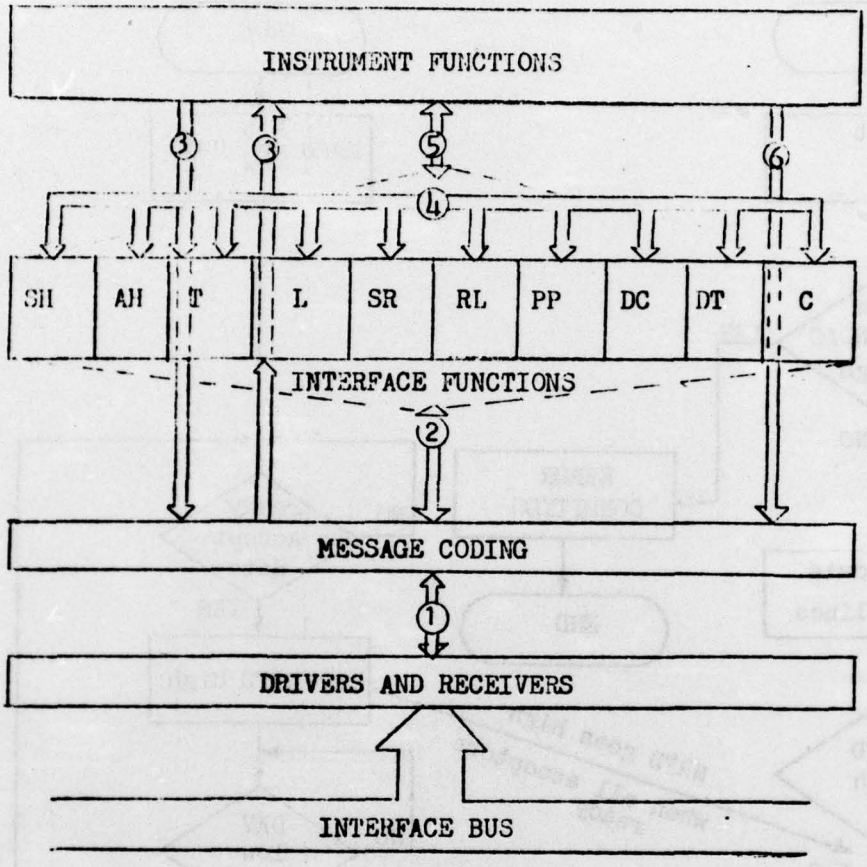


FIGURE 8 General Purpose Interface Bus (GPIB) Structure



1. Interface Bus Signal Lines
2. Remote Interface Messages to and from Instrument Functions
3. Instrument Dependent Messages to and from Instrument Functions
4. State Linkages Between Interface Functions
5. Local Messages Between Interface Functions and Instrument Functions
6. Interface Messages Sent by a Controllers Instrument Functions

FIGURE 9 Interface Functions And Instrument Message Flow Diagram

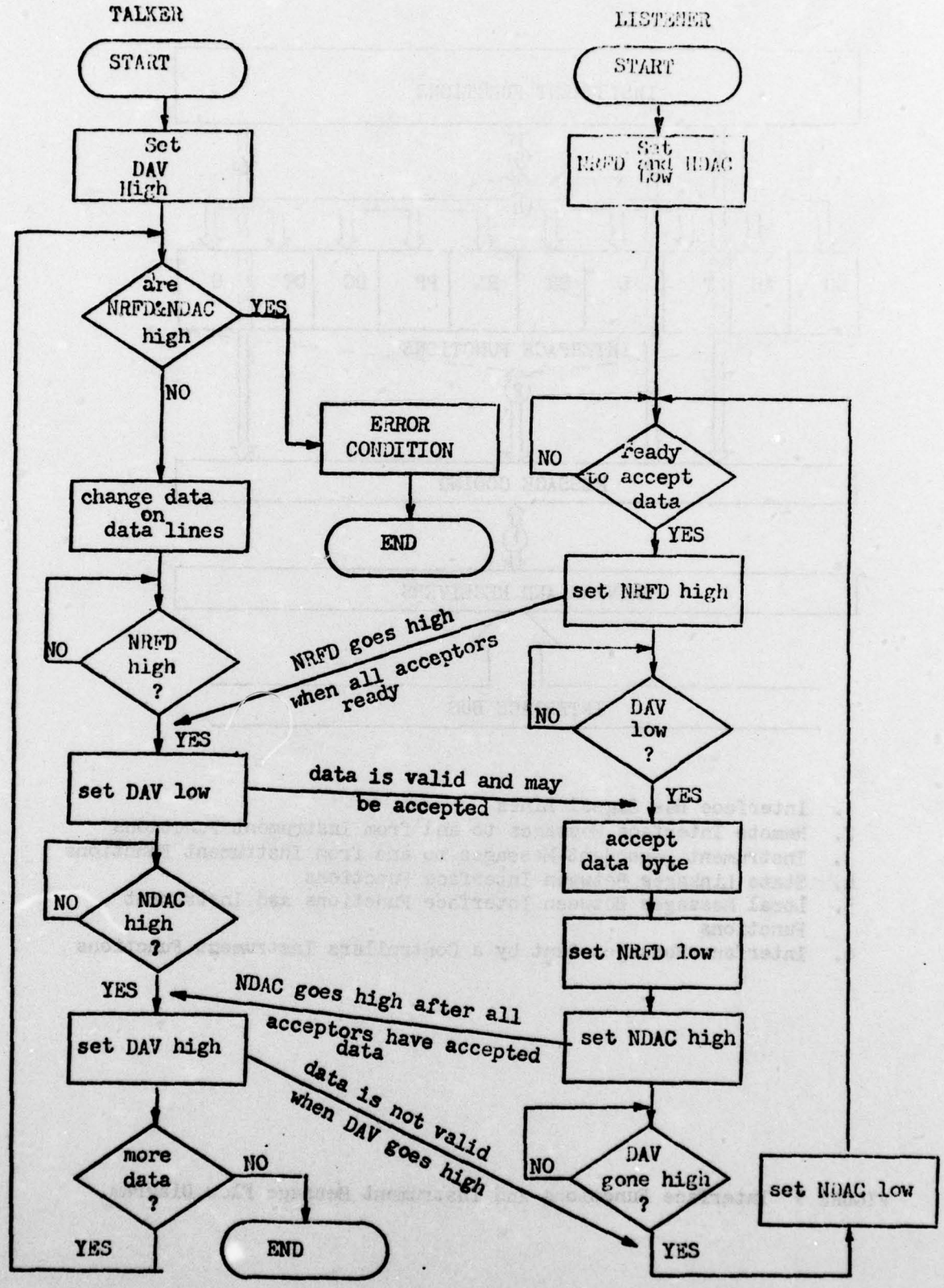


FIGURE 10 Data Transfer Using Source and Acceptor Handshake Process

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3. INTEL Corporation, INTEL 8080 Microcomputer Systems User's Manual, July 1975.

4. Institute of Electrical and Electronics Engineers IEEE Standard 488-1975

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LGMEE	1
LGMSR	1
OA	1
XPQC	1
DAPL	10
EPE	
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EET	1
EETT/DEB	1
EEIM	1
AFCS C/S	1
CCPC, Tinker AFB	6


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